Claim Amendments

Please amend claims 1, 9, and 17 as follows:

Listing of Claims

1. (currently amended) A method of forming an MIM capacitor to prevent plasma induced damage to a capacitor dielectric, comprising:

providing a substrate;

providing a capacitor opening in said substrate;

providing a bottom electrode in said capacitor opening;

thermally annealing said bottom electrode;

providing a capacitor dielectric layer in said capacitor opening on said bottom electrode; and

depositing a top electrode on said capacitor dielectric layer using a plasma-free deposition process.

2. (original) The method of claim 1 wherein said top electrode has a substantially organic-free content.

3. (original) The method of claim 1 wherein said annealing said bottom electrode comprises exposing said bottom electrode to nitrogen gas while subjecting said bottom electrode to thermal processing.

4. (original) The method of claim 3 wherein said top electrode has a substantially organic-free content.

5. (original) The method of claim 1 wherein said top electrode is deposited on said dielectric layer using a deposition temperature of no greater than about 400 degrees C.

6. (original) The method of claim 5 wherein said top electrode has a substantially organic-free content.

7. (original) The method of claim 5 wherein said annealing said bottom electrode comprises exposing said bottom electrode to nitrogen gas while subjecting said bottom electrode to thermal processing.

8. (original) The method of claim 7 wherein said top electrode has a substantially organic-free content.

9. (currently amended) A method of forming an MIM capacitor to prevent plasma induced damage to a high-K capacitor dielectric, comprising:

providing a substrate;

providing a capacitor opening in said substrate;

providing a bottom electrode in said capacitor opening;

thermally annealing said bottom electrode;

providing a high-K dielectric layer in said capacitor opening on said bottom electrode; and

depositing a top electrode on said high-K dielectric layer using a plasma-free deposition process.

10. (original) The method of claim 9 wherein said top electrode has a substantially organic-free content.

11. (original) The method of claim 9 wherein said annealing said bottom electrode comprises exposing said bottom electrode to nitrogen gas while subjecting said bottom electrode to thermal processing.

12. (original) The method of claim 9 wherein said top electrode is deposited on said dielectric layer using a deposition temperature of no greater than about 400 degrees C.

13. (original) The method of claim 9 wherein said plasma-free deposition process is a thermal chemical vapor deposition process or an atomic layer deposition process.

14. (original) The method of claim 13 wherein said top electrode has a substantially organic-free content.

15. (original) The method of claim 13 wherein said annealing said bottom electrode comprises exposing said bottom electrode to nitrogen gas while subjecting said bottom electrode to thermal processing.

16. (original) The method of claim 13 wherein said top electrode

is deposited on said dielectric layer using a deposition temperature of no greater than about 400 degrees C.

17. (currently amended) A method of forming an MIM capacitor to prevent plasma induced damage to a high-K capacitor dielectric, comprising:

providing a substrate;

providing a capacitor opening in said substrate;

providing a bottom electrode in said capacitor opening;

subjecting said bottom electrode to chemical mechanical planarization;

thermally annealing said bottom electrode;

providing a high-K dielectric layer in said capacitor opening on said bottom electrode; and

depositing a top electrode comprising TiN on said high-

K dielectric layer using a plasma-free deposition process.

18. (original) The method of claim 17 wherein said top electrode has a substantially organic-free content.

19. (original) The method of claim 18 wherein said annealing said bottom electrode comprises exposing said bottom electrode to nitrogen gas while subjecting said bottom electrode to thermal processing.

20. (original) The method of claim 19 wherein said top electrode is deposited on said dielectric layer using a deposition temperature of no greater than about 400 degrees C.